Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.071”**

**G**

**SOURCE**

**SOURCE**

**.041”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Gate Pad Size: .007 x .007”**

**Backside Potential: DRAIN**

**APPROVED BY: DK DIE SIZE .041” X .071” DATE: 10/20/21**

**MFG: SILICONIX / VISHAY THICKNESS .008” P/N: SI4431**

**DG 10.1.2**

#### Rev B, 7/1